Design in Reliability for Communication Designs

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ABSTRACT
Silicon design implementation has become increasingly complex with the deep submicron technologies such as 90nm and below. It is common to see multiple processor cores, several types of memories, I/Os, complex analog circuits and synthesized logic on the same chip. Sophisticated IP integration techniques are needed in order to realize today's complex systems-on-chip (SoC). Also, with the explosive growth in the communications semiconductor market, ensuring product reliability to meet reliability goals and achieve good yield is of significant concern. This paper is intended to bring the inherent challenges in the reliability domain and some of the effective techniques currently used in the EDA world to meet these challenges. We also discuss the need for developing new methods to address the upcoming challenges in ultra-deep submicron design environment.

Categories and Subject Descriptors
B.7.3 [Reliability and Testing]

General Terms: Design, Reliability

Keywords: Reliability, nanometer design challenges, EDA tools, Electro Migration, Self Heat

1. INTRODUCTION
The intent of this paper is to highlight the importance of reliability challenges in high volume and low power communication IC designs and highlight some of the key techniques and methodologies used in this domain. It also outlines the requirements for evolving process technologies, such as 45nm and below.

We start with focusing on various reliability challenges like IR-drop, Electro Migration (EM), Self Heat (SH), Hot electron (Hot-e), Antenna propagation, Electro Static Discharge (ESD), Gate Oxide integrity (GOX), and On chip statistical variations. Next, we describe the concept of DIR (design-in-reliability) and its importance with ultra-deep submicron design and manufacturing process. In the third section, we describe some of the design techniques to improve the reliability of the product design. Finally, we cover the current solutions available in the EDA market, methodologies associated with static and dynamic analysis flows to overcome the reliability challenges, and the current industry trends towards very deep submicron (beyond 45nm) designs. In the end, we also outline the requirements from the EDA vendors to meet the growing challenges in reliability area for evolving process nodes.

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2. RELIABILITY CHALLENGES
With ever increasing design complexities (size, clock speed, level of integration, multiple power domains etc), integrated circuit design in the sub-90nm era is a major challenge due to a variety of reliability issues. A good understanding of various reliability issues along with their impact on chip functionality and performance is very important for getting acceptable yield. In this section, we describe some of the challenges associated with reliability in sub-90nm technologies.

2.1 Power Grid IR-drop
Higher device densities and faster switching frequencies cause larger switching currents to pass through the power and ground networks resulting in IR drop. Power grid IR drop has been the primary reliability challenge since 180nm designs. Product engineers focused on accurate estimation of IR-drop on power grid at block level and full chip level. Some automated tools were available for standard logic to estimate IR-drop. Most custom blocks require significant manual effort. Traditional static IR drop is estimated using activity factors and frequency information. With increasing switching logic and usage of more low power techniques, dynamic IR drop has gained considerable attention in the recent past.

2.2 Electro Migration (EM), Self-Heat (SH):
Electro Migration is the directional migration of interconnect metal atoms caused by the flow of electrons. Increasing current density in interconnects results in Self Heating. This would result in temperature rise in interconnects, which exponentially reduces the interconnect EM time to failure. A conservative design style and building adequate design margins helped to overcome the issue on 130nm designs. Adaptation of 90nm manufacturing process technology required comprehensive EDA capabilities to design products that are EM/SH safe rather than simply over-designing with margins. Currently, they are being addressed using some static methods with worst case design parameters like activity factors, frequency and power consumption numbers. However, with ultra-deep submicron process beyond 90nm, more accurate methods are required.

2.3 Gate-Oxide, Hot-e, PMOS Negative Bias Temperature Instability(NBTI):

At 90nm technology, NBTI and hot-carrier effects cause significant P and N transistor performance degradation over device lifetime. Both effects degrade the threshold voltage (Vt) as well as the drive current (Idrive) of the P and N transistors respectively. With the advent of 65/45nm technologies, proper handling of Gate Oxide reliability, Hot Electron (Hot-e) and PMOS NBTI issues becomes more important. Currently, no viable solutions exist to mitigate these issues. Most often in-house tools are used to analyze sample blocks or some critical paths, but not at full-chip level. With these advanced processes and increasing design complexities, we need methods to analyze these at chip level.

2.4 Statistical Variations:

Designing at sub 90nm processes poses yet another challenge of handling statistical processes variations. In sub 90nm processes, random on die and wafer level variations may lead to complete circuit failure or partial failure. In the communication ICs, most often we come across System On Chip (SOC) designs containing both analog and digital component on a single die. The statistical variations can impact both analog and digital components, and care must be taken to analyze them to ensure good design performance.

3. DESIGN-IN-RELIABILITY CONCEPT

Design complexity has grown for every generation of the chip. They are driven by the rich set of features seen in current generation SoCs coupled with GHz range operating frequencies. This results in increased power consumption thus making reliability a major concern. Several low power reduction techniques such as dynamic logic, MTCMOS, switched power plane methods employed in chip design increase the complexity of reliability analysis further. Hence there is a strong need to consider reliability from the early stages of design implementation.

Traditional post silicon stress validation methods like extended life-test are no longer viable, creating significant product risk. Also the current DIR tools are too late in the design cycle and costs additional design resources and time. Traditionally reliability verification is considered to be a post silicon layout activity and many projects at Intel focused on this only for production stepping of the chip. After the functional verification on the silicon during initial stepping, subsequent steppings focused on this reliability verification activity. This caused significant rework to fix the reliability, timing and noise issues prior to production tapeouts.

This is the main reason to focus on the DIR concept where the critical reliability challenges are addressed in the chip design stage itself. Figure 1 below illustrates the DIR strategy for achieving this at the high level. This method offers to cut down significant post TO rework and made the A0 stepping as production worthy.

Intel is driving many DIR procedures to include reliability and manufacturability upstream in the design implementation cycle there by reducing the high-risk design escapes. In the recent past, EDA industry also started addressing this concept by forming a committee called SEMATECH reliability technology board. One of the key challenges is to define the DIR process and identify the major gaps from design and CAD perspectives. Another key goal is to define proper tool/methodology interface between the existing EDA tools and explore the opportunities to proliferate this concept into all design styles SOC, ASIC, Custom etc.

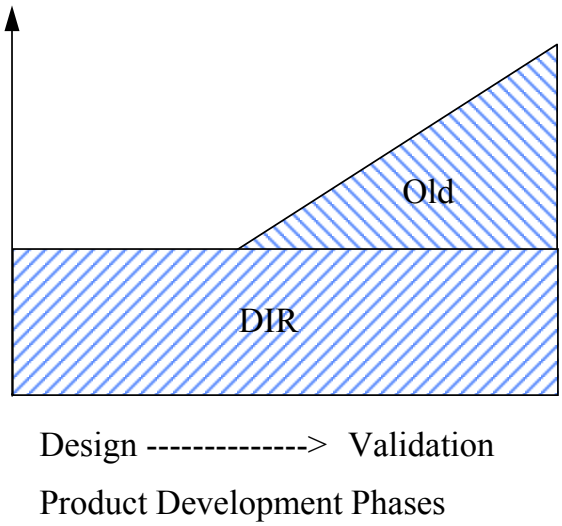


Fig1. Development trade-off with Eng efforts

Figure 2 depicts the DIR/DFM (Design for Manufacturing) process in detail and also establishes the relationship between various design stages and the reliability requirements. Correct-by-construction is a key component in the design process, where many of reliability requirements are fed into design tools/methods to produce reliability friendly design. This is primarily achieved through floorplan, place and route, early power estimators, schematic circuit analyzers etc… A DIR/DFM Cad tool is another component, where the key reliability goals are verified in the design stages before freezing the design. Path based routers, path based simulation engines, circuit aging estimation methods and signal integrity checks with reliability comprehension are few examples of this component. Primary idea is to provide the key reliability goals in the design cycle and ensure the compliance through various tools, flows and methods. It also describes about the current Gaps in the design/CAD perspective to achieve this DIR goal. Many of the solutions and methods described in this section are point tools. Lack of an integrated approach for these DIR/DFM requirements is the key industry gap.

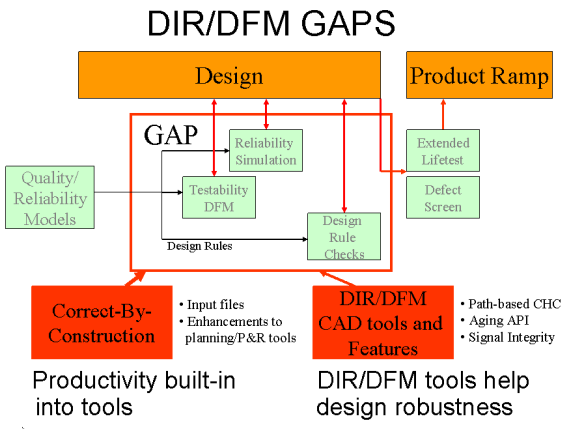


Figure 2: DIR/DFM process and key gaps.

In the following paragraphs, we will discuss some examples for DIR. Proper power grid planning at floor plan stage will provide an opportunity to meet some reliability requirements. Capability to come up with a power grid that meets IR drop and EM requirements can be incorporated at floorplan stage to reduce the iterations down in the design cycle. Also, at floor plan stage, we can drop in as many vias as possible on power grid to help achieve overall via density goals. A dynamic approach using some circuit simulators can provide enough information to estimate the current density numbers and it can be another valuable input to design reliable signal network with adequate metal/via density.

Preparing the standard cell library with key reliability goals is another salient design technique. Using the appropriate buffers with adequate drive strength and use of dynamic logic in the design stage provides another opportunity to address the DIR goals.

4. TOOLS AND METHODOLOGY FOR DIR

Intel has been working on this domain for more than a decade to come up with various CAD tools/flows and methodology using internal tools predominantly. For custom designs, EM and SH issues are addressed with static methods using worst case conditions as the post design analysis.

Same tools are expanded to work on circuits to give early estimation of current consumption there by helping the mask layout engineers to build the design margins. For SOC type designs, both the global and detailed routers are equipped with sufficient knowledge to understand the DIR requirements. We have also equipped our Parasitic Extraction flows to be friendly for reliability verification with accurate RLC extraction capabilities. Dummy fills are taken into account during capacitance extraction. For aging phenomenon, we have coupled the timing analysis engine with adequate aging estimation methods to analyze aging effects on critical paths in the design. Despite these, we found that several of these home grown solutions are inadequate as scalability of these solutions with respect to process node changes and design complexity is limited. Mature (accurate and tightly integrated) EDA vendor solutions in several areas of reliability verification is a major gap today. In order to convey the expectation from a large scale semi conductor company like Intel, in the subsequent discussion, we are providing some insight into methodologies we use for reliability verification and challenges in the domain.

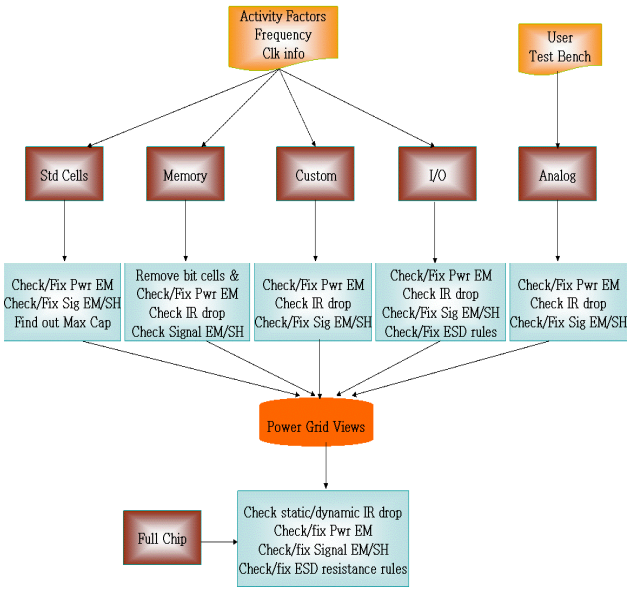
4.1 Methodological Challenges for Reliability Verification:

At Intel, we use hierarchical reliability verification methods where we divide the analysis into block level and Full-Chip (FC) level. FC is partitioned into various levels of hierarchies based on the functionality of the design. This section further describes several methodologies employed at various hierarchies such as standard cells, memories, and analog and full chip level designs. Figure 3 outlines the overall methodology.

4.2 Standard Cell and Memory EM/SH Methodology:

Checking the EMSH at the standard cell level is important as these cells will be used widely in the design. For ultra deep submicron technology, maximum capacitance of a cell is determined based on its EM/SH capability. Once a cell is designed, for EM/SH analysis, activity factors need to be carefully determined. Worst case activity factors would lead to over design, impacting the area of products designed using them. Memories pose an additional complexity in EM/SH analysis due to their size. Memories would contain mostly the bit cells (millions of devices) with little periphery logic (few thousands devices) Runtimes/Capacity is a bottle neck because of the huge number of bit cells. Validating the bit cell for the worst case EM/SH and black-boxing the bit cells provides a good alternative in getting around the capacity related issues.

Figure 3: Reliability Verification Methodology



4.3 Analog EM/SH Methodology:

Performing EM/SH using static methods do not work for analog circuits as the waveform does not have rail to rail swing. Hence, performing spice simulation is the only way to check for EM/SH on power/signal nets. Simulation based EM/SH would require unreduced parasitic extraction, and hence runtime intensive. Typical Spice runtime on a PLL block is more than a week. Having tools that can back annotate parasitics on hierarchical netlist and still be able to check for EM/SH would ease the runtime/capacity limits. Reduction needs to be applied to complete the simulation runs especially on power nets. However, identifying worst case vectors poses a major challenge and automating this is still an open problem.

4.4 Full-Chip EM/SH Methodology:

Power grid poses a different challenge. Power grid analysis at the cell level assumes all ports are connected to the voltage source. However, when they are placed in the design, some of the ports may be closer to the pads and some of those connections may be missed. This would change the entire current distribution on interconnects within the cells which would result in different EM violations. The EM violations depend on how the connections happen on the top level. Hence, we would need to include the internals of the cells when performing the block/full chip power grid analysis. As the std. cells, macros, analog blocks are already checked for EM, it makes sense to take advantage of the cell level runs. Hence, running the power grid analysis using the bottom level views created would give tremendous advantage of the run times.

The EM violations need to be carefully analyzed for power grid as few thousands of violations can go away with one metal connection. Signal net analysis can work out of using the top level runs with output transition times (from timer) and input capacitance (from .lib information). Automatic fixing the SH violations in a P&R data is very important and can really help if we use the P&R tool itself for SH analysis. Traditionally, EM was the dominant factor compared to the SH on power nets and we were checking for only EM on power nets. From 65nm, SH is becoming dominant which requires us to perform SH checks on power nets. We don't have any vendor tools to perform the power grid SH.

Coming up with activity factor (AF) for EM/SH is also getting challenging with new design methodologies. We still don't have a proper method in coming up with realistic activity factors. VCD based AF methods exist, but performing full chip simulations is tedious.

5. DIR GAPS: EDA INDUSTRY REQUIREMENTS

The following section describes the gaps in the existing EDA tools and the challenges we anticipate on future process nodes.

5.1 Temperature aware EM/SH analysis and Placement engines:

As we move towards sub-65nm technologies, EM/SH analysis is gaining importance. We observed that typically, 65nm show more EM/SH violations than 90nm designs. In case of 90nm designs, to perform EM/SH analysis, we assumed uniform (high) temperature across the chip. Due to exponential temperature dependency of current density, we used to find very high number of violations in the chip. However, this is not realistic as entire die need not operate at same temperature. It is reasonable to expect to have memory blocks at a lower temperature than a control logic block. In order to quantify this, for 65nm designs, we need to perform temperature mapping of the chip, using which we have to identify EM/SH violations in every region. This would result in eliminating some amount of pessimism, and hence helping reduction in design effort. Similarly, for automated place and route tools, placement engines can be enhanced to identify locations with possible lower power and hence temperature, place the cells in such a way that they can result in fewer EM/SH violations. Some EDA vendors now offer on-die temperature simulators which are used for timing and power analysis. If temperature solution is coupled with APR engine, we can perform accurate analysis of designs which would result in lesser number of violations.

5.2 EM/SH check capability on passive devices:

Most of the analog designs use passive devices like resistors and RF designs use inductors. As these devices are made of interconnect layers (metals/vias), we need to check for EM/SH within the device. Most of the extractors in the market don't extract the internals of these devices and the traditional EM/SH checkers will not check for the violations inside the device. As more and more RF is getting integrated onto the silicon, it would be important to have tools that would check for the EM/SH within the inductors or resistors. The tool should read the width of the resistors and apply appropriate EM/SH rules to catch violations. To handle inductors, the DSPF of the inductor with interconnect W/Ls needs to be read in by circuit simulators and check for the current density limits and flag the violations.

5.3 Statistical Variations:

In case of analog designs, random variations of threshold voltage, fluctuations in doping densities, mismatch of differential pairs, stress., etc. can result in what is called "parametric yield loss" of a circuit. Due to this it is not enough, if circuit is designed to work under nominal process and operating conditions. The design of the circuit must be robust to the statistical variations which place three important requirements for models and tools used for analog simulation (i) Compact device models used for analog simulation must include statistical device parameter variations. There is a lot of research and development happening to incorporate statistical variations in device models across the industry (ii) Simulation engines must provide capability to analyze the performance of circuit under random variations and predict the yield and (iii) we need optimization engines which can analyze the sensitivity of various performance parameters (such as gain, bandwidth, offset, ..) to the process parameters as well design parameters (W, L, ..) and allow designers to size the circuits in order to come up with robust circuit design.

In case of digital designs, random process variations manifest themselves as variations in timing characteristics of the design. Conventional approach to come up with robust designs is to use corner based static timing analysis approach where we characterize cell libraries at various PVT (Process Voltage Temperature) conditions. However, due several sources of variation libraries need to be characterized at a large number of corners which is computationally expensive. Also, in this approach, designs are optimized at very extreme corners which have low probability of occurrence. Because of this approach;, the designs are often conservative or suboptimal. As an alternative, we should consider actual statistics of process parameters and use them to compute statistical characteristics of the designed circuit to achieve less pessimistic results in efficient runtime. This approach is still emerging industry and is known as statistical static timing analysis.

5.4 Schematic and Layout Electrical Rule Checks:

Several communication products requiring high performance at lower area and power consumption include custom digital circuitry. These are normally very large blocks involving design efforts from several designers. Electrical Rule Checking is a method to check the robustness of a design both at schematic and layout levels against various "design rules". These design rules are often project specific and are developed based on past learning from silicon or in anticipation of potential failures. At schematic level examples of the rules are checking P/N device size ratio is with in the given range of product, floating devices, floating nets, connecting high voltage to thin gates, checking that lengths/widths of the devices is as per the limit specified by spice models, checking for maximum allowed series pass gates, estimation charge sharing in a domino gate, issues related to level shifter designs, .etc. Similarly at layout level several checks can be performed. We incorporate typically 100+ rules in a project to ensure robustness of circuits and layouts.

Electrical rule checkers have high significance in our wireless products where reduction in power consumption is highly important. Some of the low power techniques like shutting down the power supply using power switches provide a high reliability risk. For cells like level shifters or interface logic, turning off the input power domain can potentially create the output net to stay in

the center of the output power domain voltage creating a huge short circuit power resulting in the chip failure. In order to catch circuits that are not designed to handle these scenarios, we should have an electrical rule checker that would identify these and warn the users during design phase rather than seeing an actual silicon failure.

Currently, there are no tools in the EDA industry for schematic electrical rule checking and it is a clear gap.

5.5 Transient analysis during turn-on/turn-off of on-chip power switches operation to check for any Simultaneous switching noise at full chip:

On-chip Power switch usage is quite common in low power applications. During the power-on sequence of the power switch, there can be sudden surge in the current taken by the logic. If this current is too large and if the on-chip decoupling capacitance is limited, then there would be lots of noise on the power grid and would result in silicon failures. There are few tools in the market to perform this kind of analysis. However, because the tool needs to perform a spice simulation, the capacity is quite limited. Especially if the power switches are placed at the top level and supply power to huge blocks, performing spice simulation would be a tedious task and normally limited by the tool's capacity.

As the usage of power switches keeps growing, if the capacity of these tools can be enhanced to handle huge designs, this would improve the product reliability. The tools should also identify potential noise and automatically insert the decoupling capacitors to reduce the noise.

5.6 Performing GOX failure analysis using Overshoots/undershoots from the Signal Integrity tool:

As gate thickness decreases with each new process technology, the probability of gate oxide breakdown increases. As thermal/electrical stress increases, the gate leakage increases which ultimately leads to circuit failure. Some of the circuits like memory tend to have higher sensitivity to the GOX compared to logic. Hence, we need to consider the failure rate based on the circuit type. On logic, we need to have tools that would read the overshoots and undershoots from the Signal Integrity tool and capture any realistic failure.

5.7 ESD resistance rule checkers:

Most of the layout based ESD rules are checked using tools like Hercules. However, there are no tool to check for resistance based ESD rules between clamps and power supplies. Intel currently uses internal solution, but having an external tool for performing the resistance based ESD checks would greatly help.

6. SUMMARY AND CONCLUSIONS

Intel has been extensively performing reliability checks on communication designs. Currently, reliability CAD solutions are generally pessimistic negatively effecting overall design efficiency. Incorporation of realistic activity factors and use of statistical techniques can lead to optimal designs and design cycle times. In addition, tools which are scalable and tightly integrated are needed in order to produce reliability solutions within custom and SOC design frameworks. For our future success on 65nm and 45nm products, we look forward to see these gaps addressed by EDA industry.

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