Test Item	Description	Test Condition SPEC	Readout (Hrs)	Sampling Plan		Reference
				SS/Acc	LTPD	
ESD	Voltage step HBM : (1). step 250V, for 500V to 2500V (2). step 500V, for 2500V to 4000V MM : (1).step 25V, for 50V to 200V (2).step50V, for 200V to 400V	Human Body Model: 2000V	N/A	3/0	N/A	MIL-STD-883E 3015.7
		Machine Model: 200V	N/A	3/0	N/A	JESD22-A115
Latch-up	±100mA or actual rating; 1.5×Vcc or absolute max rating	±100mA current trigger 1.5XVcc	N/A	3/0	N/A	JESD 78
Preconditioning Test	模擬IC上板測試 濕敏感度試驗	Visual inspection	All	410/11	5%	J-STD-020C JESD22-A113
		SAT (top and bottom side) Die area 0%, Other interface<10% (註1)	30 pcs			
		Temp Cycle: –65°C to 150°C	5 Cycles			
		Bake 125°C	24			
		MST 30°C / 60%RH	192			
		Epoxy IR reflow 240(+0/-5)°C Eutectic IR reflow 240(+0/-5)°C Pb-Free IR reflow 260(+0/-5)°C	3 Times			
		SAT (top and bottom side) Die area 0%, Other interface<10% (註1)	30 pcs			

Solderability before precondition	封裝接腳之焊接性是否良好	Tsol = 235 ± 5℃(Eutectic) Tsol = 245 ± 5℃(Pb-free) Tsol means solder temperature	5 ± 0.5 sec	15/0	15%	JESD22-B102
High Temperature Operating Life Test (HTOL)	長時間高溫狀態下對工作中的IC所產生的影響	IC is operated in the maximum Supply Voltage. Ta = 150℃ or 125℃	500/1000	77/1	5%	JESD22-A108
High Temperature Storage Life Test (HTST)	長時間高溫狀態下對IC產生的影響測試	IC is stored in 150℃	500/1000	77/1	5%	JESD22-A103
Temperature Cycling (TCT)	測試封裝表面及封裝接合面在重覆高低溫差很大的衝擊下其抗力是否足夠	-65℃ ~ 150℃ (air to air) >10 Minutes Dwell Time	300/500 Cycles	77/1	5%	JESD22-A104
Thermal Shock Test (TST)(註2)	驗證IC在短時間內,IC 與封裝對溫度之劇烈變化之抗變能力	-65℃ ~ 150℃ (liquid to liquid) > 5 Minutes Dwell Time	300/500 Cycles	77/1	5%	JESD22-A106
Highly-Accelerated Temperature and Humidity Stress Test (HAST)	加速壽命試驗	Temperature: 130℃ Relative humidity: 85%	50/100	45/0	5%	JESD22-A110
Pressure Cooker Test (PCT)	為驗證封裝的抗高溫高溼高壓能力	Temperature: 121℃ Relative humidity: 100% Vapor pressure: 2 atm	96/168	45/0	5%	JESD22-A102

註 1 : SAT scan 規格與量測層別(test layer)

1. Die surface area 0% 脫層 (delamination) between die surface and compound.
2. Other interface area < 10% 脫層 (delamination).(註1-1)
   2.1 epoxy layer < 10% die backside area
   2.2 layer between top L/F and compound. < 10%
   2.3 layer between L/F backside and compound. < 10%

註 1-1: (delamination)脫層 Other interface area 內容補充說明

a. Preconditioning Test 前 delamination 必須是< 10%.方可執行驗證.

b.當 Preconditioning Test 後 delamination 是≧10%但≦30%且電測 pass 時
可將 samples 加做 baking 8 hr 後重掃 SAT.再行比較確認其差異點.
samples 做 baking 8 hr 後重掃 SAT 後 delamination< 10%.視爲良品續流程.
若>10%但≦30%時則需將此 delamination Samples(須少於 10ea)標上記號
加做 TCT-test item (300/500 Cycles)後通過電測 pass.可視爲驗證合格.
過程相關資料需於驗證報告中附註說明.

註 2: 在下列情況,產品需要執行 TST(Thermal Shock Test)認可

1. 客戶需求執行 TST 測試.
2. High power 或 high current 的產品,如 LDO, switch regulator.
3. 新的 QFP 與 DIP 封裝外包廠,需做 1 批工程批 TST 200cycles,
   並由 PE/QA 評估決定是否續做 TST.
4. 晶片的 metal 層材質變更,或尺吋變小.
5. 新的封裝型式,如 BGA, Flip Chip 等.